REMARKS

The Applicant has carefully considered this application in connection with the Examiner's Action and respectfully requests reconsideration of this application in view of the foregoing amendment and the following remarks. The Applicant originally filed Claims 1-28. Claims 1-20, 22, 23 and 26 were previously canceled without prejudice or disclaimer, and Claims 29 and 30 were previously added. The Applicant presently cancels Claims 27 and 28 without prejudice or disclaimer. Accordingly, Claims 21, 24, 25, 29 and 30 are currently pending in the present application.

I. Rejection of Claims 27 and 28 under 35 U.S.C. §112

The Examiner has rejected Claims 27 and 28 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. While the Applicant does not necessarily agree with the Examiner's rejection, Claims 27 and 28 are presently canceled without prejudice or disclaimer, solely in an effort to expedite prosecution.

II. Rejection of Claims 21, 24 and 25 under 35 U.S.C. §102

The Examiner has rejected Claims 21, 24 and 25 under 35 U.S.C. §102 (e) as being anticipated by U.S. Patent No. 6,127,260 to Huang. In support thereof, the Examiner asserts that the metal silicide 13 disclosed in Huang reads on the first interconnect metal recited in Claim 21. However, the metal silicide 13 disclosed in Huang is not an interconnect metal. Those skilled in the art understand that interconnects are layers of conductive metal that electrically couple various

integrated components and circuits of a device. In fact, the ordinary definition of an "interconnect" feature requires that the feature couple or otherwise connect two other features - it must interconnect other features. However, the metal silicide 13 in Huang does not interconnect other components or circuits. In direct contrast, the metal silicide 13 is one of the various components or features that are interconnected by an interconnect (comprising an interconnect metal structure 52), as shown in FIG. 10. Thus, the metal silicide 13 is interconnected by an interconnect metal, but the metal silicide 13 is not itself an interconnect metal.

The Examiner also asserts that the tee-shaped, lower metal plug structure 44 disclosed in Huang reads on the second interconnect metal recited in Claim 21. However, the lower metal plug structure 44 is a via, not an interconnect metal. As those skilled in the art understand, and as used in the present application, vias are metal filled openings between various layers of a semiconductor device that provide electrical connection between the layers. (Page 2, lines 7-10). The lower metal plug structure 44, in conjunction with the upper metal plug structure 50, clearly provides such electrical connection through various insulative layers (20, 24, 31, 38, 39 and 45) and between the overlying interconnect metal structure 52 and the underlying metal silicide 13. (FIG. 10). Thus, the lower metal plug structure 44 is a via, not an interconnect. Moreover, the Examiner asserts that the narrow opening 42a is a via (as discussed below), yet maintains that the lower metal plug structure 44 is an interconnect, even though the lower metal plug structure 44 is formed in the narrow opening 42a. Those skilled in the art understand that interconnect structures are not formed in vias. Accordingly, the lower metal plug structure 44 does not read on the second interconnect metal recited in Claim 21.

The Examiner also asserts that the narrow opening 42a disclosed in Huang reads on the via recited in Claim 21 of the present application. However, as discussed above, a via is a metal filled opening between various layers of a semiconductor device that provides electrical connection between the layers. In contrast, the narrow opening 42a is merely an empty opening, and does not provide electrical connection between layers in the absence of the metal plug structure 44 subsequently formed therein. Therefore, the narrow opening 42a disclosed in Huang is not a via as recited in Claim 21.

Accordingly, Huang fails to disclose each and every element recited in Claim 21 of the present application. Therefore, Huang fails to anticipate Claim 21 and its dependent Claims 24 and 25. Consequently, the Applicant requests the Examiner withdraw the §102 rejection with respect to Claims 21, 24 and 25.

III. Rejection of Claims 21, 24 and 25 under 35 U.S.C. §102

The Examiner has rejected Claims 21, 24 and 25 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,177,340 to Yoo, *et al.* ("Yoo"). In support thereof, the Examiner asserts that the titanium silicide layer 9 reads on the first interconnect metal recited in Claim 21. However, as discussed above with respect to Huang, a silicide layer comprising a portion of a gate structure is not an interconnect. Moreover, Yoo fails to disclose that the titanium silicide layer 9 is interconnected to any other component. For example, as shown in FIG. 20, the titanium silicide layer 9 remains isolated between a polysilicon layer 4, silicon nitride spacers 6 and a silicon oxide insulator layer 19. (See also, FIGs. 3 and 6). Thus, not only is the titanium silicide layer 9 not an

interconnect metal, but the titanium silicide layer 9 is not even interconnected to other components by actual interconnect structure.

The Examiner also asserts that the tungsten plug 31 disclosed in Yoo reads on the second interconnect metal recited in Claim 21 of the present application. However, as also discussed above with respect to Huang, the tungsten plug 31 is a via, not an interconnect metal. More specifically, the lower tungsten plug 31 (in conjunction with the upper tungsten plug 55) clearly provides electrical connection through various insulative layers (19, 23, 35 and 49) to a source/drain region 5a/5b. (See FIGs. 1 and 20). As such, the lower tungsten plug 31 is a via. Moreover, the Examiner asserts that the contact hole opening 27 is a via (as discussed below), yet maintains that the tungsten plug 31 is an interconnect, even though the tungsten plug 31 is formed in the contact hole opening 27. Again, those skilled in the art understand that interconnect structures are not formed in vias. Thus, the tungsten plug 31 does not read on the second interconnect metal recited in Claim 21.

The Examiner also asserts that the upper tungsten plug 55 disclosed in Yoo reads on the third interconnect metal recited in Claim 21 of the present application. However, in the same manner as discussed above regarding the lower tungsten plug 31, the upper tungsten plug is a via, not an interconnect. The upper tungsten plug 55 (in conjunction with the lower tungsten plug 31) provides electrical connection through various insulative layers (19, 23, 35 and 49) to a source/drain region 5a/5b. (See FIGs. 1 and 20), which is a function of a via and not of an interconnect.

The Examiner also asserts that the contact hole openings 27 and 51 disclosed in Yoo read on the via recited in Claim 21 of the present application. However, as discussed above with respect to Huang, a via is a metal filled opening between various layers of a semiconductor device that provides electrical connection between the layers. In contrast, the contact hole openings 27 and 51 are merely

openings, and do not provide electrical connection between layers in the absence of the tungsten plugs 31 and 55 subsequently formed therein. Therefore, the contact hole openings 27 and 51 disclosed in Huang do not read on the via recited in Claim 21.

Accordingly, Yoo fails to disclose each and every element recited in Claim 21 of the present application. Therefore, Yoo fails to anticipate Claim 21 and its dependent Claims 24 and 25. Consequently, the Applicant requests the Examiner withdraw the §102 rejection with respect to Claims 21, 24 and 25.

IV. Rejection of Claims 29 and 30 under 35 U.S.C. §102

The Examiner has rejected Claims 29 and 30 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,163,067 to Inohara, *et al.* ("Inohara"). In support thereof, the Examiner asserts that the silicide layer 25 disclosed in Inohara reads on the first metal feature recited in Claim 29. However, the silicide layer 25 is not located on a semiconductor surface, as required of the first metal feature recited in Claim 29. In contrast, the silicide layer 25 is located in source/drain regions 22a/22b. Therefore, the silicide layer 25 does not read on a first metal feature located on a semiconductor surface, as recited in Claim 29.

The Examiner also asserts that the stopper film 13a disclosed in Inohara reads on the first etch stop layer recited in Claim 29 of the present application. However, the stopper film 13a is not located on the silicide layer 25. In contrast, the stopper film 13a is located over and laterally adjacent the silicide layer 25. In fact, Inohara discloses using the stopper film 13a as a mask to form the underlying silicide layer 25, such that edges of openings in stopper film 13a coincide with the outer edges of the silicide layer 25. (Column 9, lines 52-65; column 11, lines 15-24). Accordingly, the

silicide layer 25 lies only within an opening in the stopper film 13a, such that the stopper film 13a is not located on the silicide layer 25. Therefore, the stopper film 13a does not read on a first etch stop layer located on a first metal feature, as recited in Claim 29.

The Examiner also asserts that the contact hole 32 reads on the unsegmented via recited in Claim 29. However, as discussed above with respect to Huang and Yoo, a contact hole is not a via. Again, a via is a metal filled opening between various layers of a semiconductor device that provides electrical connection between the layers. Thus, an empty, un-filled opening through multiple layers, such as the contact hole 32, is not a via.

Moreover, those skilled in the art will recognize that Inohara discloses forming a via by forming the contact hole 32 and subsequently filling the hole 32 with a conductive layer 16a and a conductive member 16b. In addition, the Examiner asserts that the conductor member 16b reads on the second metal feature recited in Claim 29 of the present application. However, the Examiner cannot assert that the single via, comprising the contact hole 32 filled with the conductive layer 16a and conductor member 16b, reads on both the unsegmented via and the second metal feature recited in Claim 29. Thus, Inohara fails to disclose either an unsegmented via or a second metal feature as recited in Claim 29. Because those skilled in the art will recognize that the contact hole 32 filled with the conductive layer 16a and conductor member 16b is a via, Inohara fails to disclose a second metal feature as recited in Claim 29.

Accordingly, Inohara fails to disclose each and every element recited in Claim 29 of the present application. Therefore, Inohara fails to anticipate Claim 29 and its dependent Claim 30. Consequently, the Applicant requests the Examiner withdraw the §102 rejection with respect to Claims 29 and 30.

V. Examiner's Response to Applicant's Arguments

The Examiner asserts that the Applicant's previous argument that the multiple silicide layers 25 disclosed in Inohara are not the same feature or interconnected is not convincing because the claimed language does not clearly state whether the first metal feature is a continuous or interconnected layer. However, the Applicant believes the Examiner misinterpreted the Applicant's argument. The Applicant was trying to convey that the silicide layers 25 do not comprise one or more interconnect metals because they do not interconnect other components. As discussed above with respect to Huang, the silicide layers 25 disclosed in Inohara are employed in the conventional manner as contacts on source/drain regions 22a/22b. Thus, the silicide layers 25 may be interconnected, but they are not interconnects. Accordingly, the Applicant respectfully traverses the Examiner's response.

VI. Conclusion

In view of the foregoing remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 21, 24, 25, 29 and 30.

The Applicant requests the Examiner telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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